AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings, labeled as Fig. 3, is newly proposed.

Attachment: Proposed sheet

REMARKS

Claims 1-7 were examined with claims 1-4 rejected and claims 5-7 objected to. Claims 1-4 have been canceled, and thus claims 5-7 are pending.

Drawings

The drawings have been objected to because the Examiner asserts that they do not show every feature of the invention specified in the claims. More specifically, the Examiner asserts that the group of memory transistors having 16 to 32 memory transistors, as recited in claim 2, is not shown in the drawings. Applicant respectfully disagrees. The drawings show that each of the groups of memory transistors includes "1 ... 16-32x", which indicates 16-32 memory transistors.

The Examiner also asserts that the means for measuring a first current, means for storing the measured first current, means for supplying a read potential, means for measuring a resulting second current, and means for comparing the second current with the stored first current, as recited in claim 6, are not shown in the drawings. Applicant has therefore provided a proposed drawing, which is labeled as Fig. 3. On the left side of the proposed drawing is a means for supplying a read potential to gate terminals of the row and column to be read 301, and on the right side is a means for measuring a first current 302, means for storing the measured first current 303, means for measuring a resulting second current 302, and means for comparing the second current with the stored first current 304. Also, the specification has been amended to include a description of this proposed drawing. No new matter has been added. If this proposed replacement drawing is accepted by the Examiner, Applicant will provide a formal drawing.

Claim Objections

The Examiner objects to claims 5-7 because the phrase "opening the selection transistor" is allegedly not clear. In response, Applicant has amended the claims to instead recite "applying a high potential to the gate terminal of the selection transistor."

Claim Rejections - 35 U.S.C. §§ 102 and 103

Claims 1 and 3 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Iwahashi (U.S. Patent No. 6,081,453), and claims 2 and 4 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwahashi in view of Park et al. (U.S. Patent No. 6,501,684).

While not conceding the validity of the prior art rejections, but merely to advance prosecution, Applicant has canceled claims 1-4, thereby rendering the prior art rejections moot.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By Laura C. Brutman

Laura C. Brutman
Registration No.: 38,395
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant

Attachment